<u>WHAT IS CLAIMED IS</u>:

We claim:

1.   A linear interpolator for interpolating a first input voltage V_{in1} and a second input

voltage V_{in2} according to a factor r, wherein $0 \leq r \leq 1$, comprising:

      a first differential pair of transistors adapted to split a differential current

proportional to V_{in1} such that a first transistor in the first differential pair conducts a

differential current proportional to $r*V_{in1}$ and a second transistor conducts a differential

current proportional to $(1-r)*V_{in1}$; and

      a second differential pair of transistors adapted to split a current proportional to

V_{in2} such that a first transistor in the second differential pair conducts a differential

current proportional to $(1-r)*V_{in2}$ and a second transistor in the second differential pair

conducts a differential current proportional to $r*V_{in2}$.

2.   The linear interpolator of claim 1, further comprising:

      a third differential pair of transistors adapted to split a differential current

proportional to $-V_{in1}$ such that a first transistor in the third differential pair conducts a

differential current proportional to $-r*V_{in1}$ and a second transistor in the third differential

pair conducts a differential current proportional to $(1-r)*V_{in1}$; and

      a fourth differential pair of transistors adapted to split a differential current

proportional to $-V_{in2}$ such that a first transistor in the fourth differential pair conducts a

differential current proportional to $-(1-r)*V_{in2}$ and a second transistor in the fourth

differential pair conducts a current proportional to $-r*V_{in2}$.

3.   The linear interpolator of claim 2, wherein the first and second transistors in the first and second differential pairs are MOS transistors.

4.   The linear interpolator of claim 2, wherein the first and second transistors in the

5   first and second differential pairs are bipolar transistors.

5.   The linear interpolator of claim 2, further comprising:

a first load coupled between a supply voltage and the first transistors in the first and second differential pairs such that the differential currents conducted by the first

10   transistors in the first and second differential pairs are supplied through the first load, thereby inducing a first voltage across the first load.

6.   The linear interpolator of claim 5, further comprising:

a second load coupled between the supply voltage and the first transistors in the

15   third and fourth differential pairs such that the differential currents conducted by the first transistors in the third and fourth differential pairs are supplied through the second load, thereby inducing a second voltage across the second resistor, and wherein the difference between the second and first voltages is proportional to $r*V_{in1} + (1-r)V_{in2}$.

20   7.   The linear interpolator of claim 6, wherein the impedances of the first and second loads are equal.

8.   The linear interpolator of claim 2, further comprising a fifth differential pair of transistors adapted to split a current such that a first transistor in the fifth differential pair

25   conducts the differential current proportional to V_{in1} that is split by the first differential pair and such that a second transistor in the fifth differential pair conducts the differential

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current proportional to -V_{in1} that is split by the third differential pair.

9.   The linear interpolator of claim 8, further comprising a sixth differential pair of transistors adapted to split a current such that a first transistor in the sixth differential pair conducts the differential current proportional to V_{in2} that is split by the second differential pair and such that a second transistor in the sixth differential pair conducts the differential current proportional to -V_{in2} that is split by the fourth differential pair.

10.   The linear interpolator of claim 9, wherein the current split by the fifth differential pair equals the current split by the sixth differential pair.

11.   A linear interpolator for interpolating a first input voltage V_{in1} and a second input voltage V_{in2} according to a factor r, wherein $0 \leq r \leq 1$, comprising:

a first differential pair adapted to split a differential current proportional to r^2 such that a first transistor in the first differential pair conducts a differential current proportional to $V_{in1}*r$ and a second transistor in the first differential pair conducts a differential current proportional to $-V_{in1}*r$; and

a second differential pair adapted to split a differential current proportional to (1-r)^2 such that a first transistor in the second differential pair conducts a differential current proportional to $V_{in2}*(1-r)$ and a second transistor in the first differential pair conducts a differential current proportional to $-V_{in2}*(1-r)$.

12.   The linear interpolator of claim 11, further comprising:

a first load coupled between a supply voltage and the first transistors in the first and second differential pairs such that the differential currents conducted by the first transistors in the first and second differential pairs are supplied through the first load,

thereby inducing a first voltage across the first load.

13. The linear interpolator of claim 12, further comprising:

a second load coupled between the supply voltage and the second transistors in the first and second differential pairs such that the differential currents conducted by the second transistors in the first and second differential pairs are supplied through the second load, thereby inducing a second voltage across the second load, and wherein the difference between the second and first voltages is proportional to $r*V_{in1} + (1-r)V_{in2}$.

14. The linear interpolator of claim 11, further comprising:

a third differential pair adapted to split a current such that a first transistor in the third differential pair conducts a differential current proportional to r and a second transistor in the third differential pair conducts a differential current proportional to (1-r).

15. The linear interpolator of claim 14, further comprising: a fourth differential pair adapted to split the differential current from the first transistor in the third differential pair such that a first transistor in the fourth differential pair conducts the differential current proportional to r^2 that is split by the first differential pair.

16. The linear interpolator of claim 15, further comprising a fifth differential pair adapted to split the differential current from the second transistor in the third differential pair such that a first transistor in the fifth differential pair conduct the differential current proportional to $(1-r)^2$ that is split by the second differential pair.